



Theory of Operation

The opto coupler inputs to this card can be configured to accept a closed contact, open contact, or voltage level to satisfy a fail-safe input condition. Also a positive or negative going pulse from a pulse transformer can be used to trip the inputs in a fail-safe manner.

Either an external or local reset generates a momentary reset pulse through the use of a one shot. A single external reset contact can be used to reset any number of interlock modules with the reset inputs in parallel.

Relay contacts are shown in a de-energized state, when all interlocks are satisfied both relays are energized. Relay KSD will change state if any input trips, also a panel mounted green LED is lit to indicate that KSD is energized. Relay KFD only changes state if one of the interlocks selected by switch 1 trips, a switch contact closed selects an interlock. A red panel mounted LED will light to indicate that KFD is in a de-energized state or trip state.

The Interlock Status output provides a remote isolated closure when an interlock is satisfied. A panel mounted green LED is also lit to indicate a satisfied interlock.

First Fault Status output is normally in an open state if there are no faults latched in. During a fault condition a hex word is generated and latched in to indicate that a first fault has been recorded by a module and what the first fault is. Bit Q0 closure indicates a first fault condition has been recorded. Bits Q1, Q2, Q3 form an octal word corresponding to status bits D0 through D7.

An output line driven by the drain of an N channel FET is provided to interconnect any number of interlock modules. If this feature is used only the first fault occurring on any one of the interconnected modules will be recorded. Bits Q1, Q2, Q3 of a module can be paralleled with the same bits of any number of other interlock modules with bit Q0 unique to identify which module the first fault occurred in. Also four panel mounted LED are provided to indicate the status of Q0, Q1, Q2, and Q3. These LEDs are only lit when a module records the first fault.

If module will not reset locally, then external reset contact is closed it needs to be momentary.

Next Generation Design: A 12 bit module is possible if a common connection is used on the status bits output. One common for D0 through D11 and another common for Q0 through Q4.

Latch to other Intk Modules

Reference to FNAL Drawing No. 3823-111-ED-330052 Sheet 3 of 17		Fermilab Particle Physics Division Engineering and Technical Teams	
Title G Zero Interlock and 1st Fault Detector			
Originator: W. Jaskierny		Size	Rev
Drawn by: W. Jaskierny		FSC# No	DWG No
Originated: 22 Jan 1997		U of Ill NPL	
Last Revision: 22 Feb 1998		Scale	
Issued 19 Jun 2002		G Zero	
		Sheet 5 of 7	